IBM System z10
Introduction and Hardware Overview

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IBM Hardware

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- Microsoft
- Linux
- ITIL

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Notes:
- Performance is in Internal Throughput Rate (ITR) ratio based on measurements and projections using standard IBM benchmarks in a controlled environment. The actual throughput that any user will experience will vary depending on considerations such as the amount of multiprogramming in the user's job stream, the I/O configuration, and the workload processed. Therefore, no assurance can be given that an individual user will achieve throughput improvements equivalent to the performance ratios stated here.
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IBM System z10 Hardware

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IBM z10 EC Continues the CMOS Mainframe Heritage

- G4 – 1st full-custom CMOS S/390®
- G5 – IEEE-standard BFP; branch target prediction
- G6 – Copper Technology (Cu BEOL)
- z900 – Full 64-bit z/Architecture®
- z990 – Superscalar CISC pipeline
- z9 EC – System level scaling
- z10 EC – Architectural extensions

GHz does matter
- It is the "rising tide that lifts all boats"
- It is especially important for CPU-intensive applications

GHz is not the only dimension that matters
- System z focus is on balanced system design across many factors
  - Frequency, pipeline efficiency, energy efficiency, cache / memory design, I/O design
  - System performance is not linear with frequency
    - Need to use LSPR + System z capacity planning tools for real client / workload sizing

System z has been on consistent path while others have oscillated between extremes
- Growing frequency steadily, with occasional jumps/step functions (G4 in 1997, z10 in 2008)

z10 leverages technology to get the most out of high-frequency design
- Low-latency pipeline
- Dense packaging (MCM) allows MRU cooling which yields more power-efficient operation
- Virtualization technology (etc.) allows consistent performance at high utilization, which makes CPU power-efficiency a much smaller part of the system/data-center power consumption picture
IBM z10 EC Instruction Set Architecture

- Continues line of upward-compatible mainframe processors
  - Application compatibility since 1964
  - Supports all z/Architecture-compliant OSes

- Rich CISC Instruction Set Architecture (ISA)
  - 894 instructions (668 implemented entirely in hardware)
  - 24, 31, and 64-bit addressing modes
  - Multiple address spaces robust inter-process security
  - Multiple arithmetic formats
  - Industry-leading virtualization support
    - High-performance logical partitioning via PR/SM™
    - Fine-grained virtualization via z/VM scales to 1000’s of images
  - Precise, model-independent definition of hardware/software interface

- Architectural extensions for IBM z10 EC
  - 50+ instructions added to improve compiled code efficiency
  - Enablement for software/hardware cache optimization
  - Support for 1 MB page frames
  - Full hardware support for Hardware Decimal Floating-point Unit (HDFU)
z10 EC Chip Relationship to POWER6™

- New Enterprise Quad Core z10 EC processor chip
- Siblings, not identical twins
- Share lots of DNA
  - IBM 65nm Silicon-On-Insulator (SOI) technology
  - Design building blocks:
    - Latches, SRAMs, regfiles, dataflow elements
    - Large portions of Fixed Point Unit (FXU), Binary Floating-point Unit (BFU), Hardware Decimal Floating-point Unit (HDFU), Memory Controller (MC), I/O Bus Controller (GX)
  - Core pipeline design style
    - High-frequency, low-latency, mostly-in-order
  - Many System z and System p® designers and engineers working together
- Different personalities
  - Very different Instruction Set Architectures (ISAs)
    - very different cores
  - Cache hierarchy and coherency model
  - SMP topology and protocol
  - Chip organization
  - IBM z10 EC Chip optimized for Enterprise Data Serving Hub

IBM System z: System Design Comparison

- System I/O Bandwidth
  - 288 GB/sec*
  - 172.8 GB/sec*
  - 96 GB/sec
  - 54 GB/sec
  - 32 GB/sec
  - 16 GB/sec
  - 8 GB/sec

- Balanced System
  - CPU, nWay, Memory, I/O Bandwidth*
  - ITR for 1-way
  - *Servers exploit a subset of its designed I/O capability
  - ** Up to 1 TB per LPAR

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The key problem of current microprocessor-systems: Memory access does not scale with CPU-cycletime!

Scalability: System-Structures optimized for data

z10-EC Systemstructure:

- Mainstorage (up to 384 GB)
- Level 2 Cache (48 MB)

2 x 6 GB/s
2 x 6 GB/s
2 x 6 GB/s
2 x 6 GB/s
2 x 6 GB/s
2 x 6 GB/s
2 x 6 GB/s
2 x 6 GB/s
2 x 6 GB/s
96 GB/s
**Machine Type**
- 2097

**Models**
- E12, E26, E40, E56 and E64

**Processor Units (PUs)**
- 17 (17 and 20 for Model E64) PU cores per book
- Up to 11 SAPs per system, standard
- 2 spares designated per system
- Dependant on the HW model - up to 12, 26, 40, 56 or 64
  PU cores available for characterization
  - Central Processors (CPs), Integrated Facility for Linux (IFLs), Internal Coupling Facility (ICFs), System z10
  Application Assist Processors (zAAPs), System z10
  Integrated Information Processor (zIIP), optional - additional System Assist Processors (SAPs)

**Memory**
- System Minimum of 16 GB
- Up to 384 GB per book
- Up to 1.5 TB for System and up to 1 TB per LPAR
  - Fixed HSA, standard
  - 16/32/48/64 GB increments

**I/O**
- Up to 48 I/O Interconnects per System @ 6 GBps each
- Up to 4 Logical Channel Subsystems (LCSSs)

**ETR Feature, standard**

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**z10 EC Overview**

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**z10 EC – Under the covers (Model E56 or E64)**

- **Internal Batteries (optional)**
- **Power Supplies**
- **2 x Support Elements**
- **3x I/O cages**
- **Processor Books, Memory, MBA and HCA cards**
- **Ethernet cables for internal System LAN connecting Flexible Service Processor (FSP) cage controller cards**
- **InfiniBand I/O Interconnects**
- **2 x Cooling Units**
z10 EC Multi-Chip Module (MCM)
- 96mm x 96mm MCM
  - 103 Glass Ceramic layers
  - 7 chip sites
  - 7356 LGA connections
  - 17 and 20 way MCMs
- CMOS 11s chip Technology
  - PU, SC, S chips, 65 nm
  - 5 PU chips/MCM – Each up to 4 cores
  - One memory control (MC) per PU chip
  - 21.97 mm x 21.17 mm
  - 994 million transistors/PU chip
  - L1 cache/PU core
    - 64 KB i-cache
  - L1.5 cache/PU core
    - 128 KB D-cache
  - L2 cache/PU core
    - 3 MB
  - 4.4 GHz
  - 0.23 ns Cycle Time
  - 6 km of wire
  - 2 Storage Control (SC) chip
    - 21.11 mm x 21.71 mm
    - 1.6 billion transistors/chip
    - L2 Cache 24 MB per SC chip (48 MB/Book)
    - L2 access to/from other MCMs
    - 3 km of wire
  - 4 SEEPROM (S) chips
    - 2 x active and 2 x redundant
    - Product data for MCM, chips and other engineering information
  - Clock Functions – distributed across PU and SC chips
    - Master Time-of-Day (TOD) and 9037 (ETR) functions on the SC

Up to Four cores per PU
- 4.4 GHz
- L1 cache/PU core
  - 64 KB I-cache
- 128 KB D-cache
- 3 MB L1.5 cache/PU core
- Each core with its own Hardware Decimal Floating Point Unit (HDFU)
- Two Co-processors (COP)
  - Accelerator engines
  - Data compression
  - Cryptographic functions
  - Includes 16 KB cache
  - Shared by two cores
- L2 Cache interface
  - Shared by all four cores
  - Even/odd line (256B) split
- I/O Bus Controller (GX)
  - Interface to fanout
  - Compatible with System z9 MBA
- Memory Controller (MC)
  - Interface to controller on memory DIMMs
z10 EC Additional Details for PU Core

- Each core is a superscalar processor with these characteristics:
  - The basic cycle time is approximately 230 picoseconds
  - Up to two instructions may be decoded per cycle
  - Maximum is two operations/cycle for execution as well as for decoding
  - Memory accesses might not be in the same instruction order
  - Most instructions flow through a pipeline with different numbers of steps for various types of instructions. Several instructions may be in progress at any instant, subject to the maximum number of decodes and completions per cycle
  - Each PU core has an L1 cache divided into a 64 KB cache for instructions and a 128 KB cache for data
  - Each PU core also has a L1.5 cache. This cache is 3MB in size. Each L1 cache has a Translation Lookaside Buffer (TLB) of 512 entries associated with it

z10 Compression and Cryptography Accelerator

- Data compression engine
  - Static dictionary compression and expansion
  - Dictionary size up to 64 KB (8K entries)
  - Local 16 KB caches for dictionary data
- CP Assist for Cryptographic Function (CPACF)
  - DES (DEA, TDEA2, TDEA3)
  - SHA-1 (160 bit)
  - SHA-2 (224, 256, 384, 512 bit)
  - AES (128, 192, 256 bit)
  - PRNG
- Accelerator unit shared by two cores
  - Independent compression engines
  - Shared cryptography engines
### z10 Hardware Decimal Floating Point Unit

- Decimal arithmetic widely used in commercial and financial applications
  - Computations often handled in software
  - Avoids rounding and other problems with binary/decimal conversions
- On IBM System z9 delivered in millicode – brought improved precision and function
- On IBM System z10 integrated on every core – giving a performance boost to execution of decimal arithmetic
- Growing industry support for hardware decimal floating point standardization
  - Open standard definition led by IBM, endorsed by key ISVs including Microsoft and SAP
  - Java BigDecimal, C#, XML, C/C++, GCC, DB2 V9, Enterprise PL/1, Assembler
- z/OS V1.9 Hardware Decimal Floating Point support requires:
  - High Level Assembler (z/OS V1.8)
  - Enterprise PL/1
  - XL C/C++ with PTF
  - Debug tool (in support of C/C++, PL/1, and HLASM)
  - dbx (in support of C/C++)
  - DB2 9 for z/OS (allows you to define DFP data in DB2)

*Bringing high performance computing benefits to commercial workloads*

### z10 EC SC Hub Chip

- Connects multiple z10 PU chips
  - 48 GB/Sec bandwidth per processor
- Shared Level 2 cache
  - 24 MB SRAM Cache
  - Extended directory
    - Partial-inclusive discipline
  - Hub chips can be paired
    - 48 MB shared cache
- Low-latency SMP coherence fabric
  - Robust SMP scaling
  - Strongly-ordered architecture
- Multiple hub chips/pairs allow further SMP scaling
z10 EC Processor/Memory/HCA and Book

- Up to 8 Hot pluggable HCA fanout cards
- Plugging rules apply and dependant on Model

z10 EC Book Layout

- Memory
- Fanout Cards
- DCA Power Supplies
- Cooling from/to MRU
**z10 EC Book Layout – Under the covers**

- **MCM**
- **Memory**
- **DCA Power Supplies**
- **MRU Connections**
- **Fanouts**
  - HCA2-O (InfiniBand)
  - FSP cards
  - HCA2-C (I/O cages)
  - MBA (ICB-4)

Note: Chart shows an example of how and where different fanouts are installed. The quantities installed will depend on the actual I/O configuration.

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**20 PU MCM Structure**

- **Memory**
  - 4 PU cores 4x3MB L1.5 COP MC, GX
  - 4 PU cores 4x3MB L1.5 COP MC, GX
  - 4 PU cores 4x3MB L1.5 COP MC, GX
  - 4 PU cores 4x3MB L1.5 COP MC, GX
- **24MB L2 SC**
- **Off-Book Interconnect**

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z10 EC – Inter Book Communications – Model E64

- The z10 EC Books are fully interconnected in a point to point topology as shown in the diagram.
- Data transfers are direct between Books via the Level 2 Cache chip in each MCM.
- Level 2 Cache is shared by all PU chips on the MCM.

z10 EC – Inter Book and I/O Communications – Models E54/E64

Note:
- HCA2-C for I/O domain
- HCA2-O for PSIFB Coupling Links
- HCA2-O LR for extended distance PSIFB Coupling Link
- MBA for ICBl-4
- Each HCA2-C and HCA2-O has 2 ports
- IFB connectivity is balanced across all installed Books
- HCA2-C and HCA2-O supports 6 GB/sec
I/O Subsystem host bus interconnect speeds in GBps

- InfiniBand I/O Bus
  - z10 2008: 6 GBps
  - STI z9 2005: 2.7 GBps
  - STI z990/2890 2003: 2 GBps
  - STI z900/z800 200x: 1 GBps

STI: Self-Timed Interconnect

Connectivity for Coupling and I/O

- Up to 8 fanout cards per book
  - Up to 16 ports per book
  - 48 Port System Maximum

- Fanout cards - InfiniBand pairs dedicated to function
  - HCA2-C fanout – I/O Interconnect
  - Supports all I/O, OSA, ISC-3 and Crypto Express2 cards in I/O cage domains
  - HCA2-O fanout – InfiniBand coupling links
  - New CHPID type – CIB for Coupling
  - Fiber optic external coupling link – 150 m
  - HCA2-O LR fanout – InfiniBand coupling links – Long Range
  - New CHPID type – CIB for Coupling
  - Fiber optic external coupling link – 10 Km (Unrepeated)

- MBA fanout (Not available on Model E64)
  - ICB-4
  - New connector and cables

Up to 16 CHPIDs – across 2 ports

- IFB
- HCA2-C
- IFB

Up to 16 CHPIDs – across 2 ports

- IFB
- HCA2-O
- IFB

2 CHPIDs – 1 per port

- STI
- MBA
- STI
z10 EC FICON Express4

- **FICON Enhancements**
  - High Performance FICON for System z (zHPF) for FICON Express4
  - Improved performance at extended distance for FICON Express4 (and FICON Express2) features
- **1, 2, 4 Gbps auto-negotiated**
- **Up to 336**
- **LX 10 KM, LX 4 KM and SX features**
  - A 10 KM LX transceiver is designed to interoperate with a 4 KM LX transceiver
- **Concurrent repair of optics**
- **Personalize as:**
  - FC
    - Native FICON
    - Channel-To-Channel (CTC)
      - z/OS, z/VM, z/VSE, z/TPF, TPF, Linux on System z
    - FCP (Fibre Channel Protocol)
      - Support of SCSI devices
        - z/VM, z/VSE, Linux on System z

FC 3321 FICON Express4 10 KM LX
FC 3324 FICON Express4 4 KM LX
FC 3322 FICON Express4 SX

z10 OSA-Express3

- **Double density of ports compared to OSA-Express2**
  - Reduced CHPIDs to manage
  - Reduced I/O slots
  - Reduced I/O cages or I/O drawers
  - Up to 96 LAN ports versus 48
- **Designed to reduce the minimum round-trip networking time between z10 BC & z10 EC systems (reduced latency)**
  - Designed to improve round trip at the TCP/IP application layer
    - OSA-Express3 10 GbE
      - 45% improvement compared to the OSA-Express2 10 GbE
    - OSA-Express3 GbE
      - 45% improvement compared to the OSA-Express2 GbE
  - Designed to improve throughput (mixed inbound/outbound)
    - OSA-Express3 10 GbE
      - 1.0 GBytes/ps @ 1492 MTU
      - 1.1 GBytes/ps @ 8992 MTU
      - 3-4 times the throughput of OSA-Express2 10 GbE
      - 0.90 of Ethernet line speed sending outbound 1506-byte frames
      - 1.25 of Ethernet line speed sending outbound 4048-byte frames

The above statements are based on OSA-Express2 performance measurements performed in a test environment on a System z10 EC and do not represent actual field measurements. Results may vary.
z10 OSA-Express3 – 10 GbE

- 10 Gigabit Ethernet LR (Long Reach) and SR (Short Reach)
  - One port per PCI-E adaptor
  - Two ports per feature
  - Small form factor connector (LC Duplex)
    - LR = Single Mode 9 micron fiber
    - SR = Multimode 50 or 62.5 micron fiber
  - Two CHPIDs, one port each
    - Type OSD (QDIO TCP/IP and Layer 2)
- New Microprocessor and hardware data router
  - Large send packet construction, inspection and routing performed in hardware instead of firmware
  - Large send for IPv4 traffic
  - Checksum offload
  - Concurrent LIC update
  - Designed to improve performance for standard (1492 byte) and jumbo frames (8992 byte)
- Up to 45% reduction in latency compared to OSA-Express2 10 GbE

z10 EC OSA-Express3 GbE – 4 ports feature

- Gigabit Ethernet LX and SX
  - Four ports per feature options
  - Two ports* per PCI-E adaptor/CHPID
    - OS PTF required to use 2nd port
  - CHPIDs support
    - OSD (QDIO TCP/IP and Layer 2)
    - OSN (OSA-Express for NCP)
  - Small form factor connector (LC Duplex)
- New microprocessor and hardware data router
  - Large send packet construction, inspection and routing performed in hardware instead of firmware
  - Large send for IPv4 traffic
  - Checksum offload
  - Concurrent LIC update
- Up to 45% reduction in latency compared to OSA-Express2 GbE

* NOTE: To use 2-Ports per PCI-E adaptor, the following is required – z/OS V1.9+, z/VM V5.2+, z/VSE V4.1+, z/TPF 1.1 PUT 4 with APARs.
If this support isn’t installed, only port zero on a PCI-E adaptor is ‘visible’ to the Operating System.
**Crypto Express²**
- Two features – 1 (z10 BC only) and 2 Coprocessor option (minimum of 2 features)
- Two configuration modes
  - Coprocessor (default)
    - Federal Information Processing Standard (FIPS) 140-2 Level 4 certified
  - Accelerator (configured from the HMC)
- Three configuration options (Two for 1 Coprocessor option)
  - Default set to Coprocessor
  - Concurrent Patch
- Secure Key AES (128, 192 and 256 bit) support
- Support for 13 through 19 Personal Account Numbers

**Dynamic Add Crypto to LPAR**
- No recycling of LPAR
- No POR required

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**Just in time capacity gives you control**
- Permanent and temporary offerings – with you in charge
  - Permanent offerings – Capacity Upgrade on Demand (CUoD), Customer Initiated Upgrade (CIU)
  - Temporary offerings include On/Off Capacity on Demand (On/Off CoD), Capacity Backup Upgrade (CBU) and a new one – Capacity for Planned Event (CPE)
- No customer interaction with IBM at time of activation
  - Broader customer ability to order temporary capacity
- Multiple offerings can be in use simultaneously
  - All offerings on Resource Link
  - Each offering independently managed and priced
- Flexible offerings may be used to solve multiple situations
  - Configurations based on real time circumstances
  - Ability to dynamically move to any other entitled configuration
- Offerings can be reconfigured or replenished dynamically
  - Modification possible even if offering is currently active
  - Some permanent upgrades permitted while temporary offerings are active
- Policy based automation capabilities
  - Using Capacity Provisioning Manager with z/OS 1.9
  - Using scheduled operations via HMC
z10 CoD Offerings

- **On-line Permanent Upgrade**
  - Permanent upgrade performed by customer (previously referred to Customer Initiated Upgrade - CIU)
- **Capacity Backup (CBU)**
  - For disaster recovery
  - Concurrently add CPs, IFLs, ICFs, zAAPs, zIIPs, SAPs
  - Pre-paid
- **Capacity for Planned Event (CPE)**
  - To replace capacity for short term lost within the enterprise due to a planned event such as a facility upgrade or system relocation
  - Predefined capacity for a fixed period of time (three days)
  - Pre-paid
- **On/Off Capacity on Demand (On/Off CoD)**
  - Production Capacity
  - Supported through software offering – Capacity Provisioning Manager (CPM)
  - Payment:
    - Post-paid or Pre-paid by purchase of capacity tokens
    - Post-paid with unlimited capacity usage
    - On/Off CoD records and capacity tokens configured on Resource Link
- **Customer Initiated Upgrade (CIU)**
  - Process/tool for ordering temporary and permanent upgrades via Resource Link
  - Permanent upgrade support:
    - Un-assignment of currently active capacity
    - Reactivation of unassigned capacity
    - Purchase of all PU types physically available but not already characterized
    - Purchase of installed but not owned memory

Protecting with IBM’s world-class Business Resiliency solutions

- Preplanning capabilities to avoid future planned outages, e.g. dynamic LPAR allocation without a system outage and plan ahead memory
- 100 available capacity settings
- Integrated enterprise level resiliency for heterogeneous data center disaster recovery management
- Policy driven flexibility to add capacity and backup processors
- Basic HyperSwap improves storage availability *
- Integrated cryptographic accelerator
- Tamper-resistant Crypto Express2 feature with enhanced secure key AES support and capability for increased Personal Account Numbers
- Audit logging on new Trusted Key Entry (TKE) 5.3 with optional Smart Card reader
- System z – the only platform that is EAL5 certified

* All statements regarding IBM future direction and intent are subject to change or withdrawal without notice, and represents goals and objectives only.
Tracking energy consumption within the infrastructure

- Resource Link provides tools to estimate server energy requirements before you purchase a new system or an upgrade.
- Has energy efficiency monitoring tool:
  - Introduced on IBM System z9 platform in April 2007.
  - Power and thermal information displayed via the System Activity Display (SAD).
- IBM Systems Director Active Energy Manager™ (AEM) for Linux on System z V3.1:
  - Offers a single view of actual energy usage across multiple heterogeneous IBM platforms within the infrastructure.
  - AEM V3.1 energy management data can be exploited by Tivoli enterprise solutions such as IBM Tivoli Monitoring, IBM Tivoli Usage and Accounting Manager, and IBM Tivoli OMEGAMON® XE on z/OS.
  - AEM V3.1 is a key component of IBM's Cool Blue™ portfolio within Project Big Green.

z10 EC 64-way offers a 15% improvement in performance per kWh over z9 EC 54-way.

Consolidation with Linux gets a “green light”

**System z servers may help customers become more energy efficient:**
- Deploy energy efficient technologies – reduce energy consumption and save floor space.

**Economics of IFLs and z/VM help to drive down the cost of IT:**
- IFLs attractively priced, have no impact on z/OS license fees, and z/VM and Linux software priced at real engine capacity.
- ‘No charge’ MES upgrades available when upgrading to new technology.

Over 2450 LINUX applications are supported on System z, 15% growth in 2008.
IBM konsolidiert verteilte Server und erzielt Einsparungen

Erwartetes Ergebnis bei IBM:
- Entschlackte Umgebung mit deutlich weniger Hardware
  - 3.900 verteilte Server-Images werden auf 15-20 System z10 konsolidiert
  - Wesentlicher Anstieg der durchschnittlichen Auslastung
- Weniger Personalkosten durch Virtualisierung
- Wesentliche Senkung der Softwareausgaben
  - 85% weniger Stellflächenbedarf im Rechenzentrum durch konsolidierte Server
  - Ermöglicht weiteres Wachstum
  - Bessere Ausnutzung der Anlagen
- 80% weniger Energieverbrauch
- Möglichkeit, mehr Anwendungen auf System z einzusetzen

$250M+ Ersparnisse in 5 Jahren

IBM Global Account (IGA) IT-Kosten
3.900 verteilte Serverworkloads
IT-Kostenstudie über 5 Jahre

<table>
<thead>
<tr>
<th>Kosten vertrieb (kumulativ)</th>
<th>Kosten Linux auf z (kumulativ)</th>
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Gesamtkosten

Wesentlich niedrigere IT-Betriebskosten

IBM System z and Cell Broadband Engine – The Vision
A ‘Marriage’ of Two Technologies that Perfectly Complement Each Other

System z and Cell Broadband Engine – The Vision
A ‘Marriage’ of Two Technologies that Perfectly Complement Each Other

Cell Blade
GS20, GS21, GS2x

Integrated and / or Networked Cell (NG)

Preserves the same programming model between Network and Integrated

Aerospace and Defense
Financial Services Sector
Chemicals and Petroleum
Digital Video Surveillance
Digital Media
Information Based Medicine
Electronic Design Automation
Exploiting System z for New Workloads

- Financial analytics - POC

**Excel Client**
Cell Task Creation Analysis

**System z Machine**
Financial Portfolio Data Serving Workload Management

**Blade System**
European Options Pricing

- Monte Carlo Simulation
- Financial Portfolio
- European Options Pricing
- Compute-Intensive Mathematical Model

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The right level of business continuity protection for your business

...GDPS family of offerings

- Continuous Availability of Data within a Data Center
- Continuous Availability / Disaster Recovery Metropolitan Region
- Disaster Recovery at Extended Distance
- Continuous Availability Regionally and Disaster Recovery Extended Distance

- Single Data Center
  - Applications remain active
  - Near-continuous availability to data
  - GDPS/PPRC HyperSwap Manager

- Two Data Centers
  - Systems remain active
  - Automated D/R across site or storage failure
  - No data loss
  - GDPS/PPRC HyperSwap Manager GDPS/PPRC

- Two Data Centers
  - Automated Disaster Recovery “seconds” of Data Loss
  - GDPS/GM GDPS/XRC

- Three Data Centers
  - Data availability
  - No data loss
  - Extended distances
  - GDPS/MGM GDPS/NxGM
Operating systems

**z/OS**
- Providing intelligent dispatching on z10 EC for performance
- Up to 64-way support
- Simplified capacity provisioning on z10 EC
- New high availability disk solution with simplified management
- Enabling extreme storage volume scaling
- Facilitating new zIIP exploitation

**Linux on System z**
- Large Page Support improves performance
- Linux CPU Node Affinity is designed to avoid cache pollution
- Software support for extended CP Assist instructions AES & SHA

**z/TPF**
- Support for 64+ processors
- Workload charge pricing
- Exploit encryption technology

**z/VSE™**
- Interoperability with Linux on System z
- Exploit encryption technology
- MWLC pricing with sub-capacity option

**z/VM**
- Consolidation of many virtual images in a single LPAR
- Enhanced management functions for virtual images
- Larger workloads with more scalability

System z – The Ultimate Virtualization Resource

- Massive, robust consolidation platform; virtualization is built in, not added on
- Up to 60 logical partitions on PR/SM; 100’s to 1000’s of virtual servers on z/VM
- Virtual networking for memory-speed communication, as well as virtual layer 2 and layer 3 networks supported by z/VM
- Most sophisticated and complete hypervisor function available
- Intelligent and autonomic management of diverse workloads and system resources based on business policies and workload performance objectives
IBM System z10 Business Class

Hardware Overview

Businesses are realizing the value of the mainframe within their IT infrastructure – and their business

- A highly utilized, virtualized, scalable, optimized resource for consolidating workloads to help lower overall operating cost and improve energy efficiency
- A highly secure enterprise data server – when your infrastructure is secure, your business is secure
- A backbone for an enterprise SOA hub to enable integration of applications and processes, and add flexibility – when your infrastructure is flexible, your business is flexible
- Integrates new workloads including Linux®, Java™ and Open Standards with demonstrably lower Total Cost of Ownership (TCO)

Today's Mainframe:
The Smart choice for an optimized, scalable, secure, resilient infrastructure
IBM z10 BC continues the CMOS Mainframe heritage

- Multiprise 2000 – 1st full-custom Mid-range CMOS S/390
- Multiprise 3000 – Internal disk, IFL introduced on midrange
- IBM eServer zSeries 900 (z800) - Full 64-bit z/Architecture®
- IBM eServer zSeries 900 (z800) - Superscalar CISC pipeline
- z9 BC - System level scaling
- z10 BC - Architectural extensions
- Higher frequency CPU

z10 BC Overview

- Machine Type
  - 2098
- Single Model – E10
  - Single frame, air cooled
  - Non-raised floor option available
- Processor Units (PUs)
  - 12 PU cores per System
  - 2 SAPs, standard
  - Zero spares when all PUs characterized
  - Up to 10 PUs available for characterization
    - Central Processors (CPUs), Integrated Facility for Linux (IFLs), Internal Coupling Facility (ICFs), System z10 Application Assist Processors (zAAPs), System z10 Integrated Information Processor (zIIP), optional - additional System Assist Processors (SAPs)
- Memory
  - System Minimum of 4 GB
  - Up to 128 GB for System, including HSA (up to 256 GB, June 30, 2009)
  - 8 GB Fixed HSA, standard
  - Up to 120 GB for customer use (up to 248 GB, June 30, 2009)
  - 4, 8 and 32 GB increments (32 GB increment, June 30, 2009)
- I/O
  - Up to 12 I/O Interconnects per System @ 6 Gbps each
  - 2 Logical Channel Subsystems (LCSSs)
  - Fiber Quick Connect for ESCON and FICON LX
  - New OSA-Express3 Features
  - ETR feature, standard
Two new types of Single Chip Modules (SCMs)

Processor – PU (4 SCM’s x 3 cores = 12 PU’s)

System Controller – SC (2)
### z10 BC PU/SC SCM Components

**PU Chip**
- 50mm x 50mm in size – fully assembled
- Quad core chip with 3 active cores
- 4 PU SCMs per System with total of 12 cores
- PU Chip size 21.97 mm x 21.17 mm

**SC Chip**
- 61mm x 61mm in size – fully assembled
- 2 SC SCMs per System
- 24 MB L2 cache per chip
- SC Chip size 21.11 mm x 21.71 mm

- CPC Drawer with 4 PU SCMs, 2 SC SCMs

**Assembled SCM with heatsink**
- PU Chip
- LGA

### z10 BC SCM Vs z10 EC MCM Comparison

#### z10 BC SCMs
- **PU SCM**
  - 50mm x 50mm in size – fully assembled
  - Quad core chip with 3 active cores
  - 4 PU SCMs per System with total of 12 cores
  - PU Chip size 21.97 mm x 21.17 mm

- **SC SCM**
  - 61mm x 61mm in size – fully assembled
  - 2 SC SCMs per System
  - 24 MB L2 cache per chip
  - SC Chip size 21.11 mm x 21.71 mm

#### z10 EC MCM
- **MCM**
  - 96mm x 96mm in size
  - 5 PU chips per MCM
    - Quad core chips with 3 or 4 active cores
    - PU Chip size 21.97 mm x 21.17 mm
  - 2 SC chips per MCM
    - 24 MB L2 cache per chip
    - SC Chip size 21.11 mm x 21.71 mm

- Unlabeled MCMs for System

Single PU Chip without heatsink

Single SC Chip without heatsink
z10 BC CPC Drawer Components

- Up to 32 DIMMS
- 4 x PU and 2 x SC pluggable SCMs
- PU chip, SC chips, Land Grid Array (LGA) socket, Indium foil

DCA Power
I/O Hub for fanout slots
2 x OSC/ETR Cards

z10 BC Oscillator/ETR Cards

- Oscillator/ETR Cards (2 in 1 function)
  - Quantity 2
- Mother card
  - OSC-Function
- Daughter card:
  - ETR Function/Interface
  - MT-RJ Connector for Sysplex Timer®
  - BNC connector for Pulse Per Second (PPS)

Port for Sysplex Timer
z10 BC Sub-capacity Processor Granularity

- The z10 BC has 26 CP capacity levels (26 x 5 = 130)
  - Up to 5 CPs at any capacity level
    - All CPs must be the same capacity level
- The one for one entitlement to purchase one zAAP and/or one zIIP for each CP purchased is the same for CPs of any speed.
  - All specialty engines run at full speed
  - Processor Unit Value for IFL = 120

<table>
<thead>
<tr>
<th>Number of z10 BC CPs</th>
<th>Base Ratio</th>
<th>Ratio z9 BC to z10 BC</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 CP</td>
<td>z9 BC Z01</td>
<td>1.40</td>
</tr>
<tr>
<td>2 CPs</td>
<td>z9 BC Z02</td>
<td>1.36</td>
</tr>
<tr>
<td>3 CPs</td>
<td>z9 BC Z03</td>
<td>1.30</td>
</tr>
<tr>
<td>4 CPs</td>
<td>z9 BC Z04</td>
<td>1.28</td>
</tr>
<tr>
<td>5 CPs</td>
<td>z9 BC Z04</td>
<td>1.54</td>
</tr>
</tbody>
</table>

1-way (sub-capacity 26 MIPs)

1-way 673 MIPs

FULL size Specialty Engine

z10 BC Upgrade Paths

- Can enable dynamic and flexible capacity growth for mainframe servers
- Temporary capacity upgrade available through On/Off Capacity on Demand
- Temporary, nondisruptive addition of CP processors, IFLs, ICFs, zAAPs or zIIPs
- New options for reconfiguring specialty engines if the business demands it
- New options for changing On/Off CoD configurations
- Subcapacity CBU engines

Full upgrades within the z10 BC
Any to any upgrade from the z9 BC
Any to any upgrade from z990
No charge MES upgrades on IFLs, zAAPs and zIIPs
z10 BC System Power

- z10 BC maximum configuration calculated AC input power (Statistical Maximum)
  - All systems should draw less power than this
  - Typical systems will draw less power than this

<table>
<thead>
<tr>
<th></th>
<th>1 I/O Drawer</th>
<th>2 I/O Drawers</th>
<th>3 I/O Drawers</th>
<th>4 I/O Drawers</th>
</tr>
</thead>
<tbody>
<tr>
<td>normal room (&lt;28 degC)</td>
<td>3.686 kW</td>
<td>4.542 kW</td>
<td>5.308 kW</td>
<td>6.253 kW</td>
</tr>
<tr>
<td>warm room (&gt;=28 degC)</td>
<td>4.339 kW</td>
<td>5.315 kW</td>
<td>6.291 kW</td>
<td>7.266 kW</td>
</tr>
</tbody>
</table>

- 30 Amp plug capacity (208 VAC)
  - 5.5 kW single phase or unbalanced 3 phase
    - Supports up to 2 I/O drawers
  - 8.9 kW balanced 3 phase
    - Supports all system configurations – have balanced 3 phase feature
    - Plug 2 additional BPR’s per side

Noch Fragen?

Danke!